Fig. 1 PRIOR ART

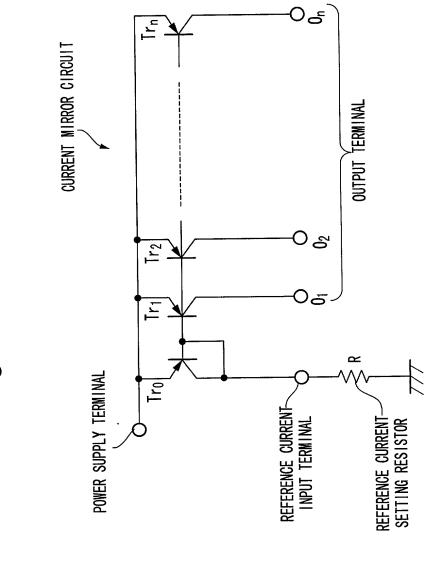
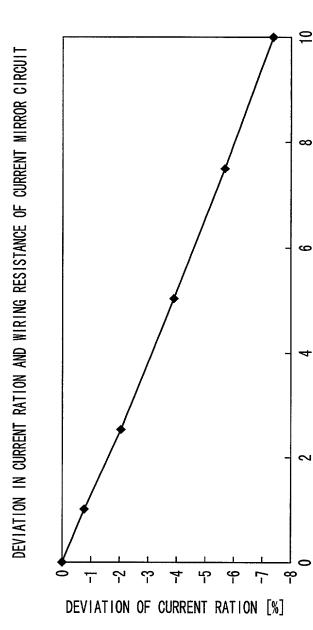


Fig. 2 PRIOR ART



UNIT WIRING RESISTANCE [Q/CELL]

Fig. 3A PRIOR ART

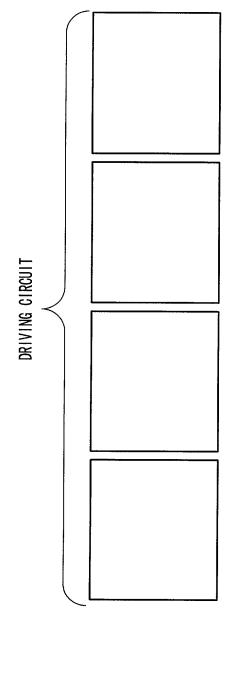
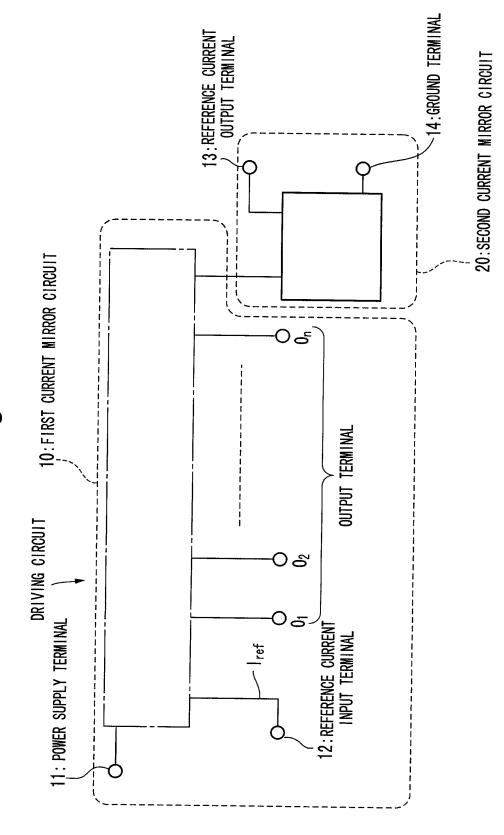


Fig. 3B PRIOR ART

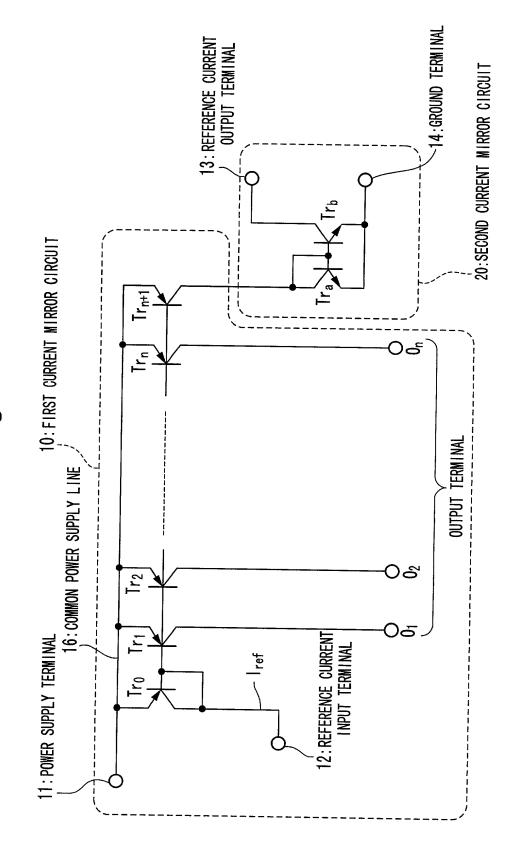


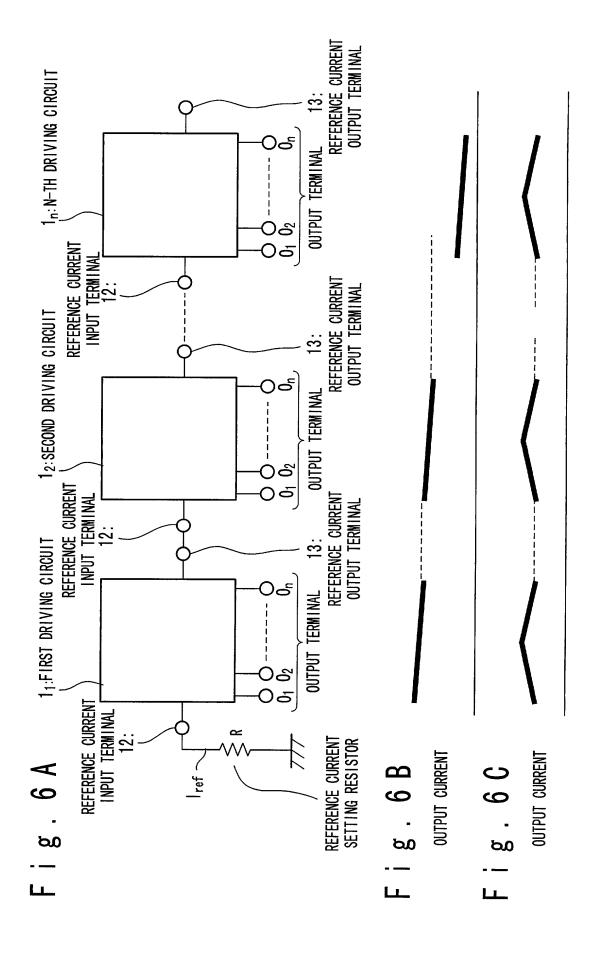
OUTPUT CURRENT

F i g . 4

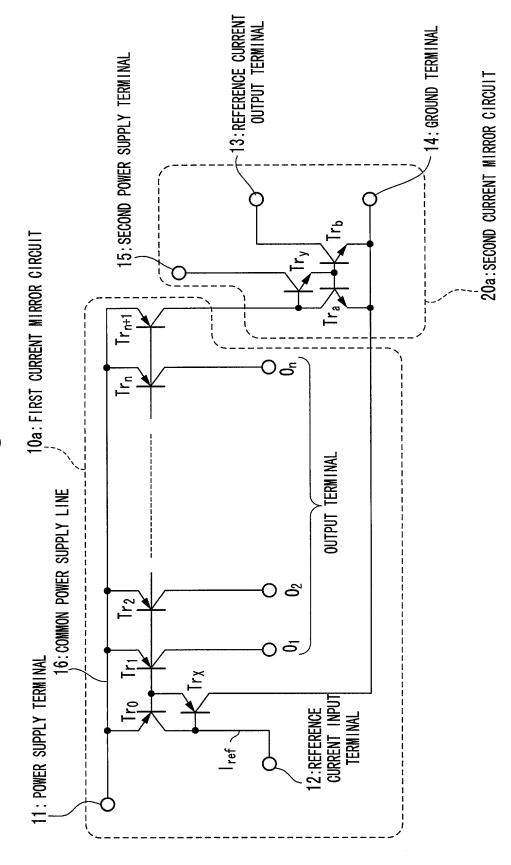


F i g . 5

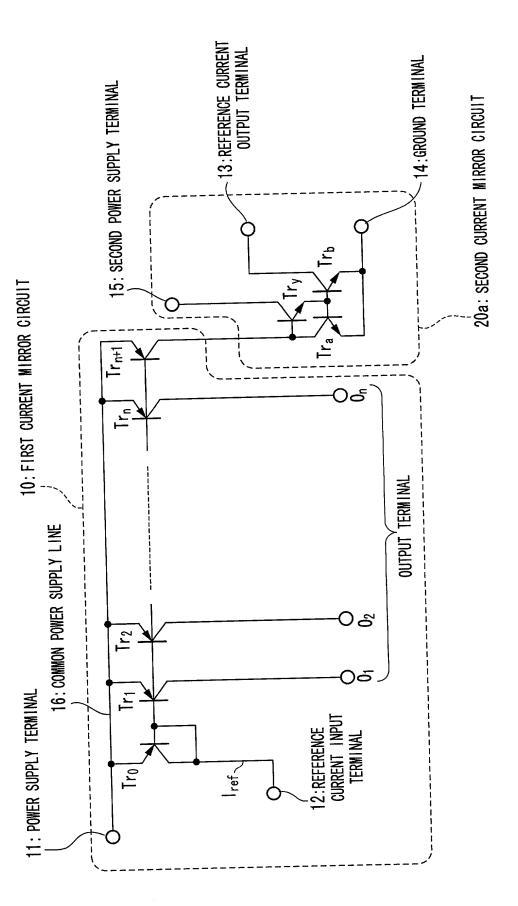




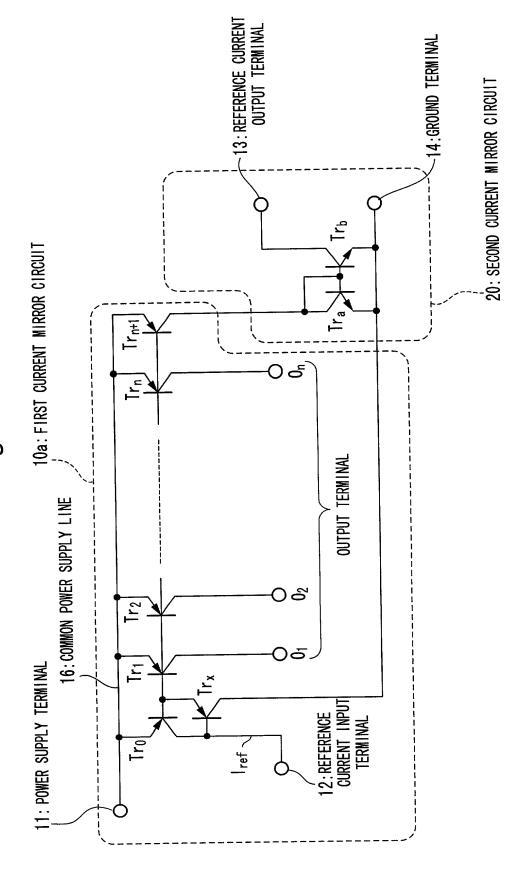
F i g . 7



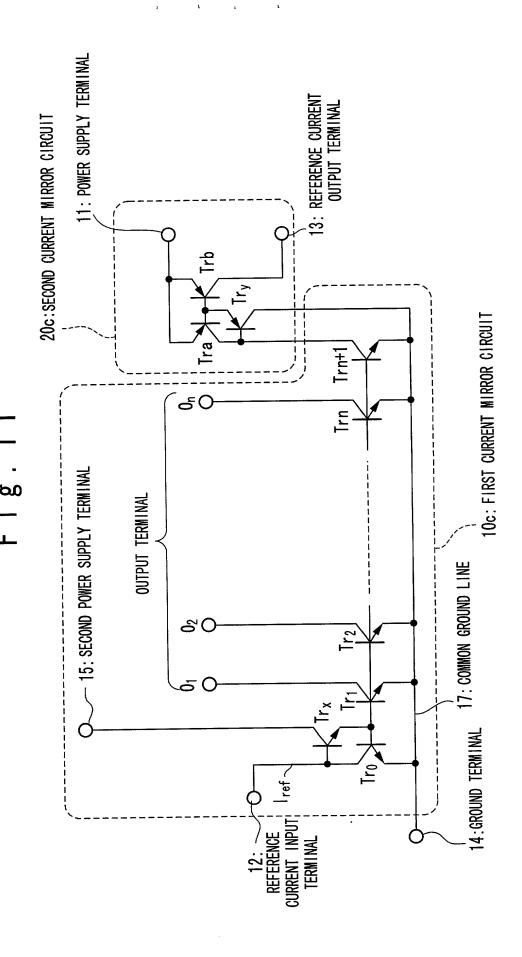
. by .—.

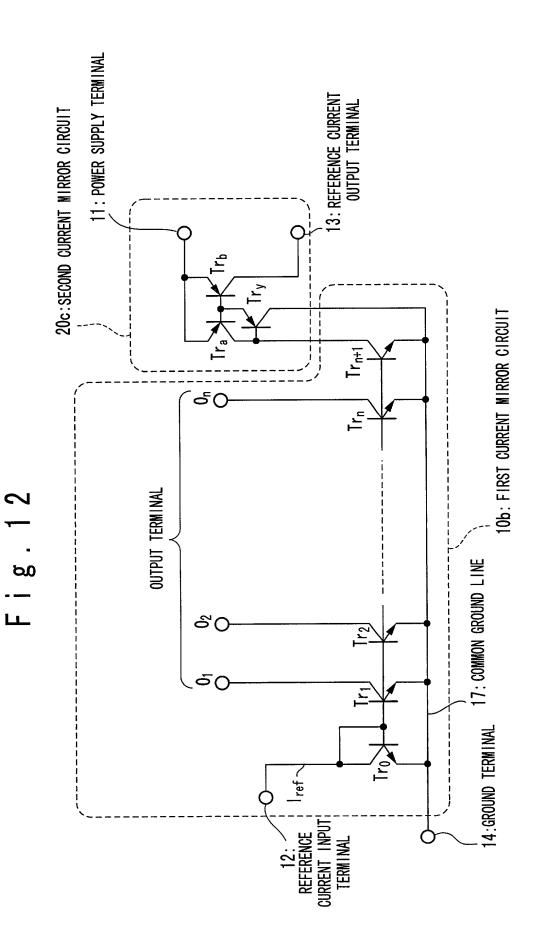


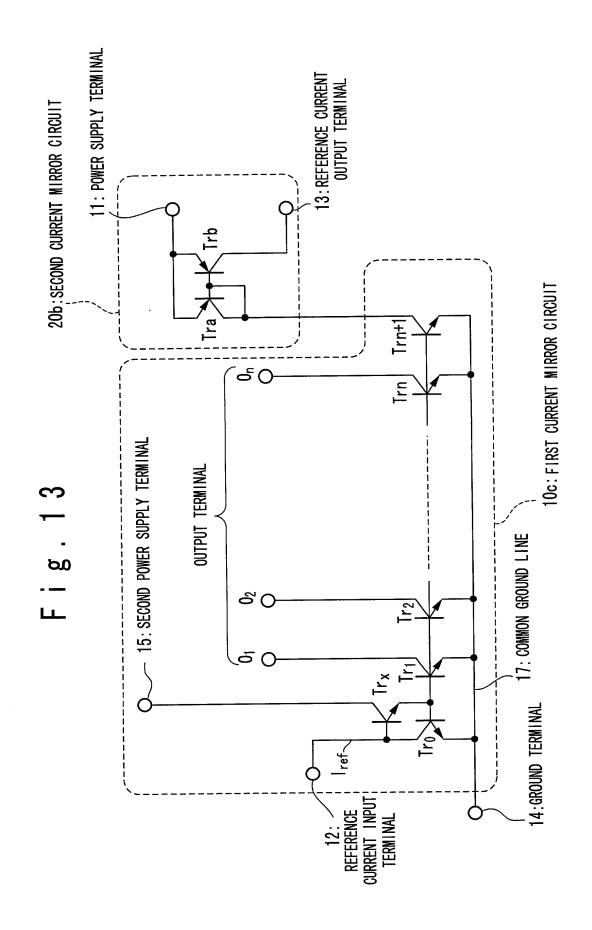
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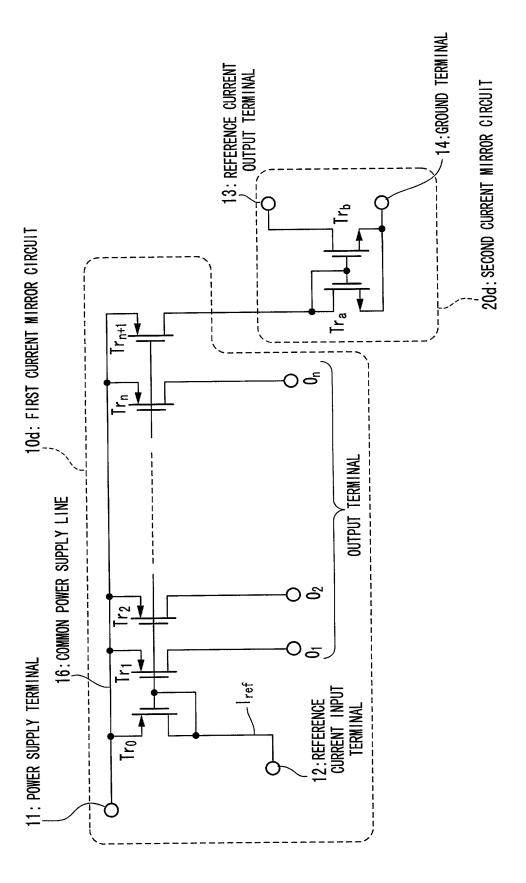
11: POWER SUPPLY TERMINAL 13:REFERENCE CURRENT OUTPUT TERMINAL 20b: SECOND CURRENT MIRROR CIRCUIT 10b: FIRST CURRENT MIRROR CIRCUIT  $\Gamma_{n+1}$ . യ — — OUTPUT TERMINAL 17: COMMON GROUND LINE 80  $\mathsf{Tr}_2$ 12:REFERENCE )CURRENT INPUT TERMINAL 14:GROUND TERMINAL Tr<sub>0</sub>/

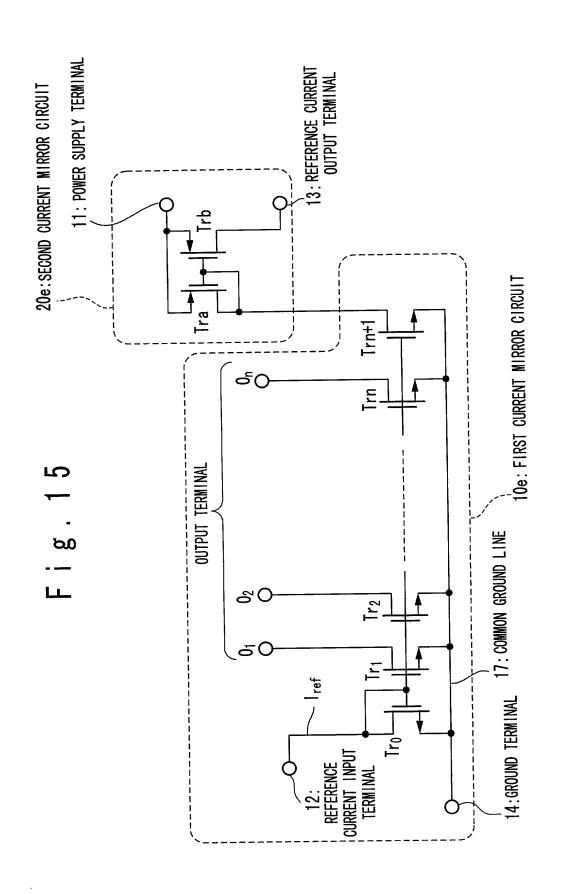






F . 8 . 1 4





F . g . 16

